INCH-POUND

MIL-M-38510/763A
7 November 1994
SUPERSEDING
MIL-M-38510/763
19 November 1990

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, ADVANCED CMOS,
COUNTERS, MONOLITHIC SILICON, POSITIVE LOGIC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, advanced CMOS, logic microcircuits. Two product assurance classes and a choice of case outlines, lead finishes, and radiation hardness assurance (RHA) are provided and are reflected in the complete Part or Identifying Number (PIN). The PIN shall be formulated in accordance with MIL-M-38510.

1.2 Classification.

1.2.1 Device types. The device types shall be as follows:

Device type	Circuit
01	To be included at a later date
02	4-bit binary counter, asynchronous reset, synchronous load
03	To be included at a later date
04	4-bit binary counter, synchronous reset and load
05	Synchronous 4-bit binary up/down counter, asynchronous load
06	To be included at a later date
07	To be included at a later date
08	To be included at a later date
09	To be included at a later date
10	To be included at a later date
11	To be included at a later date
12	To be included at a later date
13	To be included at a later date

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
2	C-2 (20 terminal, .358" x .358" x .100"), square chip carrier package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Laboratory (RL/ERDS), Griffiss AFB, NY 13441-5700, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A
FSC 5962

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK})	±20 mA
DC output current (I_{OUT})	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND})	±50 mA times the number of outputs
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C
Case operating temperature (T_C)	-55°C to +125°C

1.4 Recommended operating conditions. 2/ 3/ 4/

Supply voltage range (V_{CC})	+3.0 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Input low (V_{IL}) maximum voltage	0.90 V dc at V_{CC} = 3.0 V dc 1.35 V dc at V_{CC} = 4.5 V dc 1.65 V dc at V_{CC} = 5.5 V dc
Input high (V_{IH}) minimum voltage	2.10 V dc at V_{CC} = 3.0 V dc 3.15 V dc at V_{CC} = 4.5 V dc 3.85 V dc at V_{CC} = 5.5 V dc
Input rise and fall rate (t_r,t_f) maximum:	8 ns/V at V_{CC} = 3.6 V dc, 5.5 V dc

Minimum setup time, Pn to CP, $\overline{PL}$ (t_s)	Device type:	02	04	05	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		11.0	13.5	3.5	ns
T_C = +125°C		16.0	17.0	4.0	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		7.5	8.5	2.5	ns
T_C = +125°C		10.5	11.0	3.0	ns

Minimum hold time, Pn from CP, $\overline{PL}$ (t_h)	Device type:	02	04	05	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		0.0	0.0	1.0	ns
T_C = +125°C		0.5	0.0	1.5	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		1.5	0.0	2.0	ns
T_C = +125°C		1.5	0.0	2.0	ns

Minimum setup time, $\overline{PE}$, U/D to CP (t_s)	Device type:	02	04	05	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		11.5	12.5	9.0	ns
T_C = +125°C		15.0	16.0	10.5	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		7.5	8.0	6.0	ns
T_C = +125°C		10.5	9.5	7.5	ns

Minimum hold time, $\overline{PE}$, U/D from CP (t_h)	Device type:	02	04	05	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		0.0	0.0	0.0	ns
T_C = +125°C		0.0	0.0	0.0	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		0.0	0.0	1.0	ns
T_C = +125°C		0.0	0.0	1.0	ns

Minimum setup time, CEP, CET, $\overline{CE}$ to CP (t_s)	Device type:	02	04	05	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		6.0	6.5	7.0	ns
T_C = +125°C		7.5	8.0	9.0	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		4.5	4.5	5.0	ns
T_C = +125°C		5.5	5.5	6.0	ns

1.4 Recommended operating conditions - Continued. 2/ 3/ 4/

Minimum hold time, CEP, CET, $\overline{CE}$ from CP (t_h)	Device type:	02	04	05	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		1.0	0.0	0.0	ns
T_C = +125°C		1.0	0.0	0.0	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		1.0	0.0	0.5	ns
T_C = +125°C		1.0	0.5	0.5	ns

Minimum setup time, $\overline{SR}$ to CP (t_s)	Device type:	04	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		14.0	ns
T_C = +125°C		17.0	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		9.5	ns
T_C = +125°C		12.0	ns

Minimum hold time, $\overline{SR}$ from CP (t_h)	Device type:	04	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		0.0	ns
T_C = +125°C		0.0	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		0.0	ns
T_C = +125°C		0.0	ns

Minimum pulse width, load and count, CP (t_w)	Device type:	02	04	05	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		5.0	5.0	5.0	ns
T_C = +125°C		5.0	5.0	6.0	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		5.0	5.0	5.0	ns
T_C = +125°C		5.0	5.0	6.0	ns

Minimum pulse width, low, $\overline{MR}$, $\overline{PL}$ (t_w)	Device type:	02	05	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		5.0	5.0	ns
T_C = +125°C		5.0	5.0	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		5.0	5.0	ns
T_C = +125°C		5.0	5.0	ns

Minimum recovery time, $\overline{MR}$, $\overline{PL}$ to CP (t_{rec})	Device type:	02	05	Unit
V_{CC} = 3.0 V; T_C = +25°C, -55°C		1.5	1.0	ns
T_C = +125°C		1.5	1.5	ns
V_{CC} = 4.5 V; T_C = +25°C, -55°C		1.5	1.0	ns
T_C = +125°C		2.0	1.0	ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2/ Unless otherwise specified, all voltages are referenced to GND.

3/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back up systems. Data retention implies no input transitions and no stored data loss with the following conditions: $V_{IH} \geq 70$ percent of V_{CC}, $V_{IL} \leq 30$ percent of V_{CC}, $V_{OH} \geq 70$ percent of V_{CC} at -20 µA, $V_{OL} \leq 30$ percent of V_{CC} at 20 µA.

4/ Unless otherwise specified, the values listed above shall apply over the full V_{CC} and T_C recommended operating range.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 20 - Standard for description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

JEDEC Standard No. 17 - A Standardized Test Procedure for the characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations which prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.1.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.1.2 Truth tables. The truth tables shall be as specified on figure 2.

3.1.3 Block Diagrams. The block diagrams shall be as specified on figure 3.

3.1.4 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 4.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
High level output voltage 3006	V_{OH1} 3/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All	3.0 V	1,2,3	2.9		V
	V_{OH2} 3/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$ $V_{IL} = 1.35\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All	4.5 V	1,2,3	4.4		
	V_{OH3} 4/5/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All	5.5 V	1,2,3	5.4		
			M	02,05		1	5.4		
			D				5.4		
			R				5.4		
	V_{OH4} 3/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -4\ mA$		All	3.0 V	1,2,3	2.4		
	V_{OH5} 4/5/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$ $V_{IL} = 1.35\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$		All	4.5 V	1,2,3	3.7		
			M	02,05		1	3.7		
			D				3.7		
			R				3.7		
	V_{OH6} 3/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$		All	5.5 V	1,2,3	4.7		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$, $3.0\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
High level output voltage 3006	V_{OH7} 4/5/6/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ mA$		All	5.5 V	1,2,3	3.85		V
			M	02,05		1	3.85		
			D				3.85		
			R				3.85		
Low level output voltage 3007	V_{OL1} 3/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$		All	3.0 V	1,2,3		0.1	V
	V_{OL2} 3/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$ $V_{IL} = 1.35\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$		All	4.5 V	1,2,3		0.1	
	V_{OL3} 4/5/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$		All	5.5 V	1,2,3		0.1	
			M	02,05		1		0.1	
			D					0.1	
			R					0.1	
	V_{OL4} 3/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 12\ mA$		All	3.0 V	1,3		0.4	
						2		0.5	
	V_{OL5} 4/5/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$ $V_{IL} = 1.35\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 24\ mA$		All	4.5 V	1,3		0.4	
						2		0.5	
			M	02,05		1		0.4	
			D					0.4	
			R					0.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$, $3.0\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Low level output voltage 3007	V_{OL6} 3/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}, $V_{IH} = 3.85\ V$, $V_{IL} = 1.65\ V$; For all other inputs $V_{IN} = V_{CC}$ or GND; $I_{OL} = 24\ mA$		All	5.5 V	1,3		0.4	V
						2		0.5	
	V_{OL7} 4/5/6/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}, $V_{IH} = 3.85\ V$, $V_{IL} = 1.65\ V$; For all other inputs $V_{IN} = V_{CC}$ or GND; $I_{OL} = 50\ mA$		All	5.5 V	1,2,3		1.65	
			M	02,05		1		1.65	
			D					1.65	
			R					1.65	
Positive input clamp voltage 3022	V_{IC+} 4/5/	V_{CC} = GND; For input under test $I_{IN} = 1\ mA$		All	GND	1	0.4	1.5	V
			M	02,05			0.4	1.5	
			D				0.4	1.5	
			R				0.4	1.5	
Negative input clamp voltage 3022	V_{IC-} 4/5/	V_{CC} = Open; For input under test $I_{IN} = -1\ mA$		All	Open	1	-0.4	-1.5	V
			M	02,05			-0.4	-1.5	
			D				-0.4	-1.5	
			R				-0.4	-1.5	
Input current high 3010	I_{IH} 4/5/	For input under test $V_{IN} = V_{CC}$; For all other inputs $V_{IN} = V_{CC}$ or GND		All	5.5 V	1		0.1	µA
						2		1.0	
			M	02,05		1		0.1	
			D					0.1	
			R					0.1	
Input current low 3009	I_{IL} 4/5/	For input under test V_{IN} = GND; For all other inputs $V_{IN} = V_{CC}$ or GND		All	5.5 V	1		-0.1	µA
						2		-1.0	
			M	02,05		1		-0.1	
			D					-0.1	
			R					-0.1	
Input capacitance 3012	C_{IN}	See 4.4.1c; T_C = +25°C		All	GND	4		10.0	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ -55°C ≤ T_C ≤ +125°C 3.0 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/ Min	Limits 1/ Max	Unit
Power dissipation capacitance	C_{PD} 7/	T_C = +25°C See 4.4.1c		02,04	5.0 V	4		65	pF
				05				85	
Quiescent supply current outputs high 3005	I_{CCH} 4/5/	For all inputs V_{IN} = V_{CC} or GND		All	5.5 V	1		2.0	µA
						2		40.0	
			M	02,05		1		15	
			D					75	
			R					700	
Quiescent supply current outputs low 3005	I_{CCL} 4/5/	For all inputs V_{IN} = V_{CC} or GND		All	5.5 V	1		2.0	µA
						2		40.0	
			M	02,05		1		15	
			D					75	
			R					700	
High level ground bounce noise	V_{GBH} 8/9/	V_{LD} = 2.5 V, I_{OH} = -24 mA V_{IN} = 4.5 V or 0.0 V See figure 4		02,04	4.5 V	4		2000	mV
				05				1000	
Low level ground bounce noise	V_{GBL} 8/9/	V_{LD} = 2.5 V, I_{OL} = 24 mA V_{IN} = 4.5 V or 0.0 V See figure 4		02,04	4.5 V	4		2000	mV
				05				1000	
Latch-up input/ output over-voltage	I_{CC} (O/V1) 10/	t_w ≥ 100 µs t_{cool} ≥ t_w 5 µs ≤ t_r ≤ 5 ms 5 µs ≤ t_f ≤ 5 ms V_{test} = 6.0 V V_{CCO} = 5.5 V V_{over} = 10.5 V		All	5.5 V	2		200	mA
Latch-up input/ output positive over-current	I_{CC} (O/I1+) 10/	t_w ≥ 100 µs t_{cool} ≥ t_w 5 µs ≤ t_r ≤ 5 ms 5 µs ≤ t_f ≤ 5 ms V_{test} = 6.0 V V_{CCO} = 5.5 V $I_{trigger}$ = +120 mA		All	5.5 V	2		200	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/ Min	Limits 1/ Max	Unit
Latch-up input/ output negative over-current	I_{CC} (O/I1-) 10/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCO} = 5.5\ V$ $I_{trigger} = -120\ mA$		All	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 10/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCO} = 5.5\ V$ $V_{over} = 9.0\ V$		All	5.5 V	2		100	mA
Truth table test output voltage 3014	4/ 5/ 11/	$V_{IH} = 2.50\ V$ $V_{IL} = 0.45\ V$ verify output V_O	M	02,05	3.0 V	7	L	H	
			D				L	H	
			R				L	H	
		$V_{IH} = 3.70\ V$ $V_{IL} = 0.60\ V$ verify output V_O		All	4.5 V	7,8	L	H	
Maximum clock frequency 3003	f_{MAX} 12/	$C_L = 50\ pF$ $R_L = 500\Omega$ see figures 5 and 6		All	3.0 V	9,11	70		MHz
						10	55		
				02	4.5 V	9,11	95		
						10	80		
				04		9,11	95		
						10	90		
				05		9,11	90		
						10	80		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Propagation delay time, CP to Qn (PE input high or low) 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		02,04	3.0 V	9,11	1.0	12.0	ns
						10	1.0	14.0	
				05		9,11	1.0	13.0	
						10	1.0	16.5	
			M	02		9	1.0	12.0	
				05			1.0	13.0	
			D	02			1.0	12.0	
				05			1.0	13.0	
			R	02			1.0	12.0	
				05			1.0	13.0	
		C_L = 50 pF R_L = 500Ω see figures 5 and 6		02,04	4.5 V	9,11	1.0	8.5	ns
						10	1.0	10.0	
				05		9,11	1.0	10.0	
						10	1.0	12.0	
			M	02		9	1.0	8.5	
				05			1.0	10.0	
			D	02			1.0	8.5	
				05			1.0	10.0	
			R	02			1.0	8.5	
				05			1.0	10.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ -55°C ≤ T_C ≤ +125°C 3.0 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Propagation delay time, CP to TC 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		02,04	3.0 V	9,11	1.0	14.0	ns
						10	1.0	18.0	
				05		9,11	1.0	15.5	
						10	1.0	19.5	
			M	02		9	1.0	14.0	
				05			1.0	15.5	
			D	02			1.0	14.0	
				05			1.0	15.5	
			R	02			1.0	14.0	
				05			1.0	15.5	
		C_L = 50 pF R_L = 500Ω see figures 5 and 6		02,04	4.5 V	9,11	1.0	10.5	ns
						10	1.0	13.0	
				05		9,11	1.0	11.5	
						10	1.0	14.5	
			M	02		9	1.0	10.5	
				05			1.0	11.5	
			D	02			1.0	10.5	
				05			1.0	11.5	
			R	02			1.0	10.5	
				05			1.0	11.5	
Propagation delay time, CET to TC 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		02,04	3.0 V	9,11	1.0	11.5	ns
						10	1.0	13.5	
			M	02		9	1.0	11.5	
			D	02			1.0	11.5	
			R	02			1.0	11.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Propagation delay time, CET to TC 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		02,04	4.5 V	9,11	1.0	8.5	ns
						10	1.0	10.5	
			M	02		9	1.0	8.5	
			D	02			1.0	8.5	
			R	02			1.0	8.5	
Propagation delay time, MR to Qn 3003	t_{PHL} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		02	3.0 V	9,11	1.0	11.5	ns
						10	1.0	14.0	
			M	02		9	1.0	11.5	
			D	02			1.0	11.5	
			R	02			1.0	11.5	
		C_L = 50 pF R_L = 500Ω see figures 5 and 6		02	4.5 V	9,11	1.0	8.5	ns
						10	1.0	10.5	
			M	02		9	1.0	8.5	
			D	02			1.0	8.5	
			R	02			1.0	8.5	
Propagation delay time, MR to TC 3003	t_{PHL} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		02	3.0 V	9,11	1.0	15.0	ns
						10	1.0	18.5	
			M	02		9	1.0	15.0	
			D	02			1.0	15.0	
			R	02			1.0	15.0	
		C_L = 50 pF R_L = 500Ω see figures 5 and 6		02	4.5 V	9,11	1.0	11.5	ns
						10	1.0	14.0	
			M	02		9	1.0	11.5	
			D	02			1.0	11.5	
			R	02			1.0	11.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Propagation delay time, CP to RC 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	$C_L = 50\ pF$ $R_L = 500\Omega$ see figures 5 and 6		05	3.0 V	9,11	1.0	11.5	ns
						10	1.0	14.0	
			M	05		9	1.0	11.5	
			D	05			1.0	11.5	
			R	05			1.0	11.5	
		$C_L = 50\ pF$ $R_L = 500\Omega$ see figures 5 and 6		05	4.5 V	9,11	1.0	9.0	ns
						10	1.0	10.5	
			M	05		9	1.0	9.0	
			D	05			1.0	9.0	
			R	05			1.0	9.0	
Propagation delay time, CE to RC 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	$C_L = 50\ pF$ $R_L = 500\Omega$ see figures 5 and 6		05	3.0 V	9,11	1.0	11.5	ns
						10	1.0	14.0	
			M	05		9	1.0	11.5	
			D	05			1.0	11.5	
			R	05			1.0	11.5	
		$C_L = 50\ pF$ $R_L = 500\Omega$ see figures 5 and 6		05	4.5 V	9,11	1.0	8.0	ns
						10	1.0	10.0	
			M	05		9	1.0	8.0	
			D	05			1.0	8.0	
			R	05			1.0	8.0	
Propagation delay time, U/D to RC 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	$C_L = 50\ pF$ $R_L = 500\Omega$ see figures 5 and 6		05	3.0 V	9,11	1.0	12.5	ns
						10	1.0	15.0	
			M	05		9	1.0	12.5	
			D	05			1.0	12.5	
			R	05			1.0	12.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ 3.0 V $\le V_{CC} \le$ 5.5 V unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Propagation delay time, U/D to RC 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		05	4.5 V	9,11	1.0	9.0	ns
						10	1.0	11.0	
			M	05		9	1.0	9.0	
			D	05			1.0	9.0	
			R	05			1.0	9.0	
Propagation delay time, U/D to TC 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		05	3.0 V	9,11	1.0	11.0	ns
						10	1.0	14.0	
			M	05		9	1.0	11.0	
			D	05			1.0	11.0	
			R	05			1.0	11.0	
		C_L = 50 pF R_L = 500Ω see figures 5 and 6		05	4.5 V	9,11	1.0	8.5	ns
						10	1.0	10.5	
			M	05		9	1.0	8.5	
			D	05			1.0	8.5	
			R	05			1.0	8.5	
Propagation delay time, Pn to Qn 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		05	3.0 V	9,11	1.0	13.5	ns
						10	1.0	16.5	
			M	05		9	1.0	13.5	
			D	05			1.0	13.5	
			R	05			1.0	13.5	
		C_L = 50 pF R_L = 500Ω see figures 5 and 6		05	4.5 V	9,11	1.0	9.0	ns
						10	1.0	11.5	
			M	05		9	1.0	9.0	
			D	05			1.0	9.0	
			R	05			1.0	9.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ 3.0 V $\le V_{CC} \le$ 5.5 V unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Propagation delay time, PL to Qn 3003	t_{PHL}, t_{PLH} 4/5/ 13/14/	C_L = 50 pF R_L = 500Ω see figures 5 and 6		05	3.0 V	9,11	1.0	14.0	ns
						10	1.0	18.0	
			M	05		9	1.0	14.0	
			D	05			1.0	14.0	
			R	05			1.0	14.0	
		C_L = 50 pF R_L = 500Ω see figures 5 and 6		05	4.5 V	9,11	1.0	10.0	ns
						10	1.0	12.5	
			M	05		9	1.0	10.0	
			D	05			1.0	10.0	
			R	05			1.0	10.0	

1/ Each input/output, as applicable shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.

b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.

c. All I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

Additional detailed information on qualified devices (i.e., pin for pin conditions and testing sequence) is available from the qualifying activity (DESC-EQM) upon request. For negative and positive voltage and current values: The sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

TABLE I. Electrical performance characteristics - Continued.

2/ The word "All" in the device type column, means the value listed in the limit columns apply for all device types listed herein. Where M, D and R in the conditions column are postirradiation limits for those device types specified in the device type column.

3/ This test is guaranteed, if not tested, to the limits specified in table I.

4/ RHA samples do not have to be tested at -55°C and +125°C prior to irradiation.

5/ When performing postirradiation electrical measurements for RHA level, T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C.

6/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum.

7/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$. The dynamic current consumption, $I_S = (C_{PD} + C_L) V_{CC} f + I_{CC}$. For both P_D and I_S, f is the frequency of the input signal.

8/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} maximum = i.e., ±24 mA) and 50 pF of load capacitance (see figure 3). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse (t_r = t_f = 3.5 ±1.5 ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F. E. T. oscilloscope probe with at least 1 MΩ impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (see figure 3). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.

9/ When used in asynchronous TTL compatible systems, ground bounce (V_{GBH} and V_{GBL}) = 2,000 mV can be a possible problem.

10/ See JEDEC STD. 17 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$ and V_{over}, are to be accurate within ±5 percent.

11/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional test shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L < 2.5 V; high inputs = 3.7 V and low inputs = 0.6 V for V_{CC} = 4.5 V and H ≥ 1.5 V, L < 1.5 V; high inputs = 2.5 V and low inputs = 0.45 V for V_{CC} = 3.0 V. Tests at V_{CC} = 3.0 V are for RHA specified devices only (T_A = +25°C ±5°C). Functional tests at V_{CC} = 3.0 V are the worst case for RHA specified devices.

12/ This test is required only for Group A testing, see 4.4.1 herein.

13/ Devices are tested at V_{CC} = 3.0 V and V_{CC} = 4.5 V at T_C = +125°C for sample testing and at V_{CC} = 3.0 V and V_{CC} = 4.5 V at T_C = +25°C for screening. Other voltages of V_{CC} and temperatures are guaranteed, if not tested, see 4.4.1d.

14/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

Device types	02		04		05	
Case outlines	E, F	2	E, F	2	E, F	2
Terminal number	Terminal symbol					
1	$\overline{MR}$	NC	$\overline{SR}$	NC	P1	NC
2	CP	$\overline{MR}$	CP	SR	Q1	P1
3	P0	CP	P0	CP	Q0	Q1
4	P1	P0	P1	P0	$\overline{CE}$	Q0
5	P2	P1	P2	P1	U/D	$\overline{CE}$
6	P3	NC	P3	NC	Q2	NC
7	CEP	P2	CEP	P2	Q3	U/D
8	GND	P3	GND	P3	GND	Q2
9	$\overline{PE}$	CEP	$\overline{PE}$	CEP	P3	Q3
10	CET	GND	CET	GND	P2	GND
11	Q3	NC	Q3	NC	PL	NC
12	Q2	$\overline{PE}$	Q2	$\overline{PE}$	TC	P3
13	Q1	CET	Q1	CET	RC	P2
14	Q0	Q3	Q0	Q3	CP	PL
15	TC	Q2	TC	Q2	P0	TC
16	V_{CC}	NC	V_{CC}	NC	V_{CC}	NC
17	---	Q1	---	Q1	---	RC
18	---	Q0	---	Q0	---	CP
19	---	TC	---	TC	---	P0
20	---	V_{CC}	---	V_{CC}	---	V_{CC}

NC = No connection

Terminal symbol	Description	Applicable device type
$\overline{MR}$	Asynchronous master reset input	02
CP	Clock pulse input (timing input)	02, 04, 05
CEP	Count enable parallel input	02, 04
CET	Count enable trickle input	02, 04
$\overline{P0}$-P3	Parallel data inputs	02, 04, 05
$\overline{PE}$	Parallel enable inputs	02, 04
$\overline{Q0}$-Q3	Flip-flop outputs	02, 04, 05
$\overline{CE}$	Count enable input	05
$\overline{PL}$	Asynchronous parallel load input	05
$\overline{U/D}$	Up/down count control input	05
RC	Ripple clock output	05
$\overline{TC}$	Terminal count output	02, 04, 05
$\overline{SR}$	Synchronous reset input	04

FIGURE 1. Terminal connections.

Device types 02 and 04

$\overline{MR}$ or $\overline{SR}$ *	$\overline{PE}$	CET	CEP	Action on rising clock edge (↑)
L	X	X	X	Reset (Clear) **
H	L	X	X	Load (Pn to Qn) **
H	H	H	H	Count (Increment) **
H	H	L	X	No change (Hold) **
H	H	X	L	No change (Hold) **

* $\overline{MR}$ and $\overline{SR}$ apply to device type 02 and 04, respectively. When MR = L, the device outputs are reset independent of the clock. A reset operation supercedes any other device operation, including the "no change" operation.

** The functionality of the TC output shall satisfy the following Boolean Logic equation:

$$TC = CET \cdot Q0 \cdot Q1 \cdot Q2 \cdot Q3$$

For hold and asynchronous reset operations, the functionality of TC is independent of the clock.

Device type 05

Mode select table

$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	Mode
H	L	L	↑	Count up ***
H	L	H	↑	Count down ***
L	X	X	X	Preset (Async.) ***
H	H	X	X	No change (hold) ***

*** The functionality of the TC output shall satisfy the following Boolean Logic equation:

$$TC = (\overline{U}/D \cdot Q0 \cdot Q1 \cdot Q2 \cdot Q3) + (\overline{U}/D \cdot \overline{Q0} \cdot \overline{Q1} \cdot \overline{Q2} \cdot \overline{Q3})$$

Device type 05

$\overline{RC}$ truth table

$\overline{PL}$	$\overline{CE}$	TC*	CP	$\overline{RC}$
H	L	H	↓_↑	↓_↑
H	H	X	X	H
H	X	L	X	H
L	X	X	X	H

* TC is generated internally.

↓_↑ = Low clock pulse
H = High voltage level
L = Low voltage level
X = Irrelevent
↑ = Transition from Low-to-High voltage level

FIGURE 2. Truth tables.

DEVICE TYPE 02

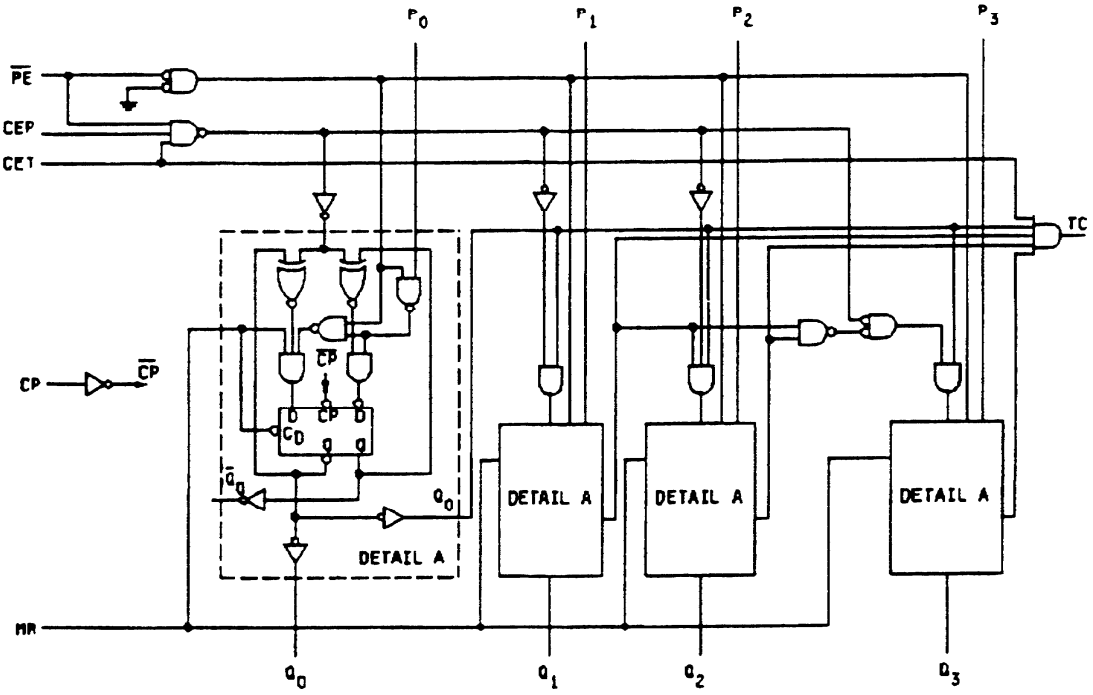


FIGURE 3. Block diagrams.

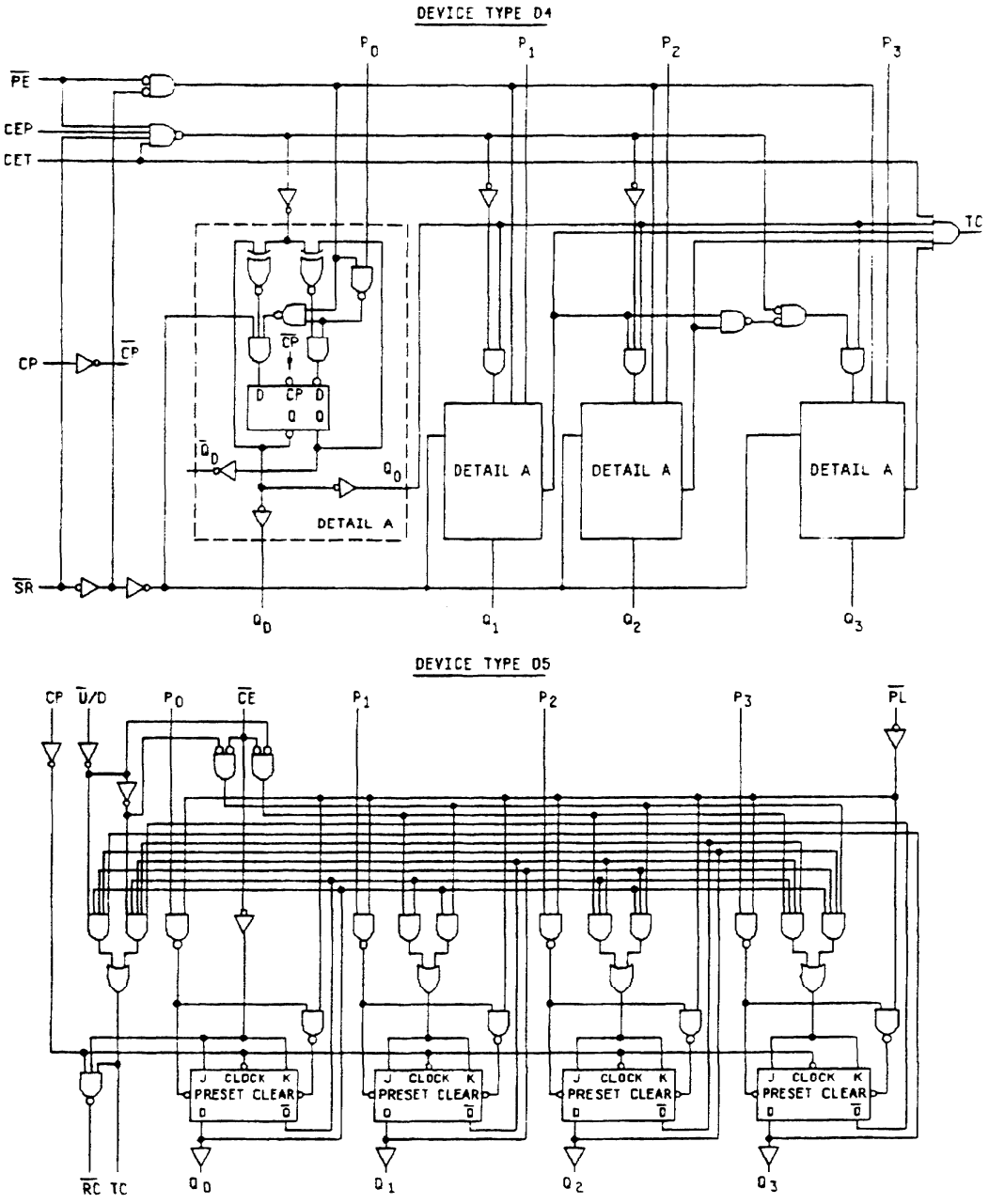
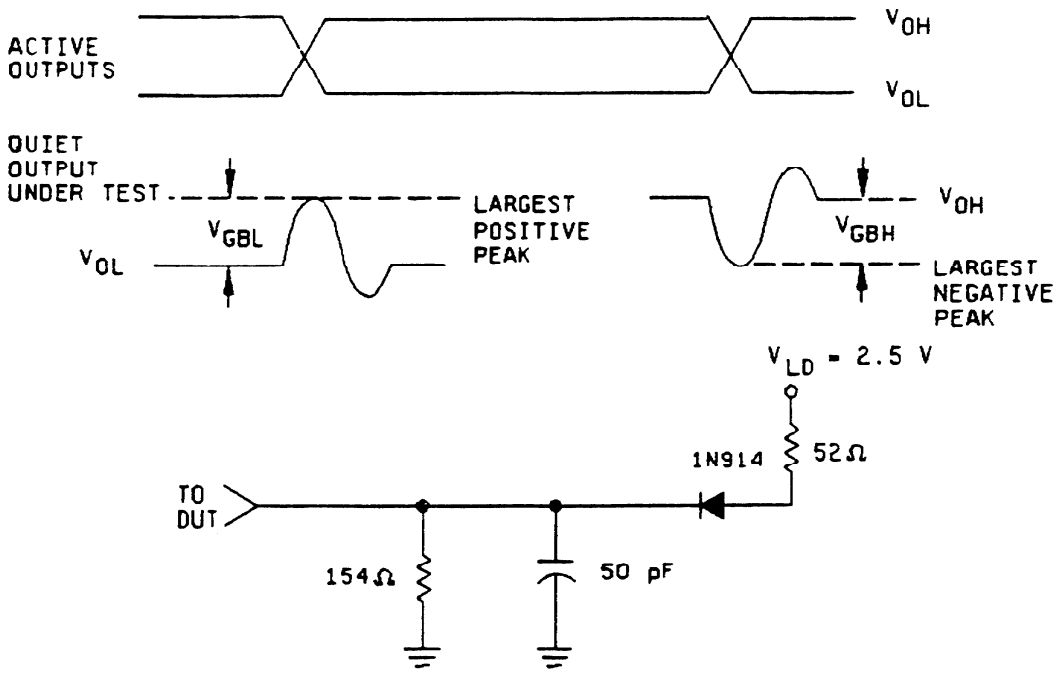


FIGURE 3. Block diagrams - Continued.



NOTE: Resistor and capacitor tolerances = ±10 %

FIGURE 4. Voltage levels for ground bounce.

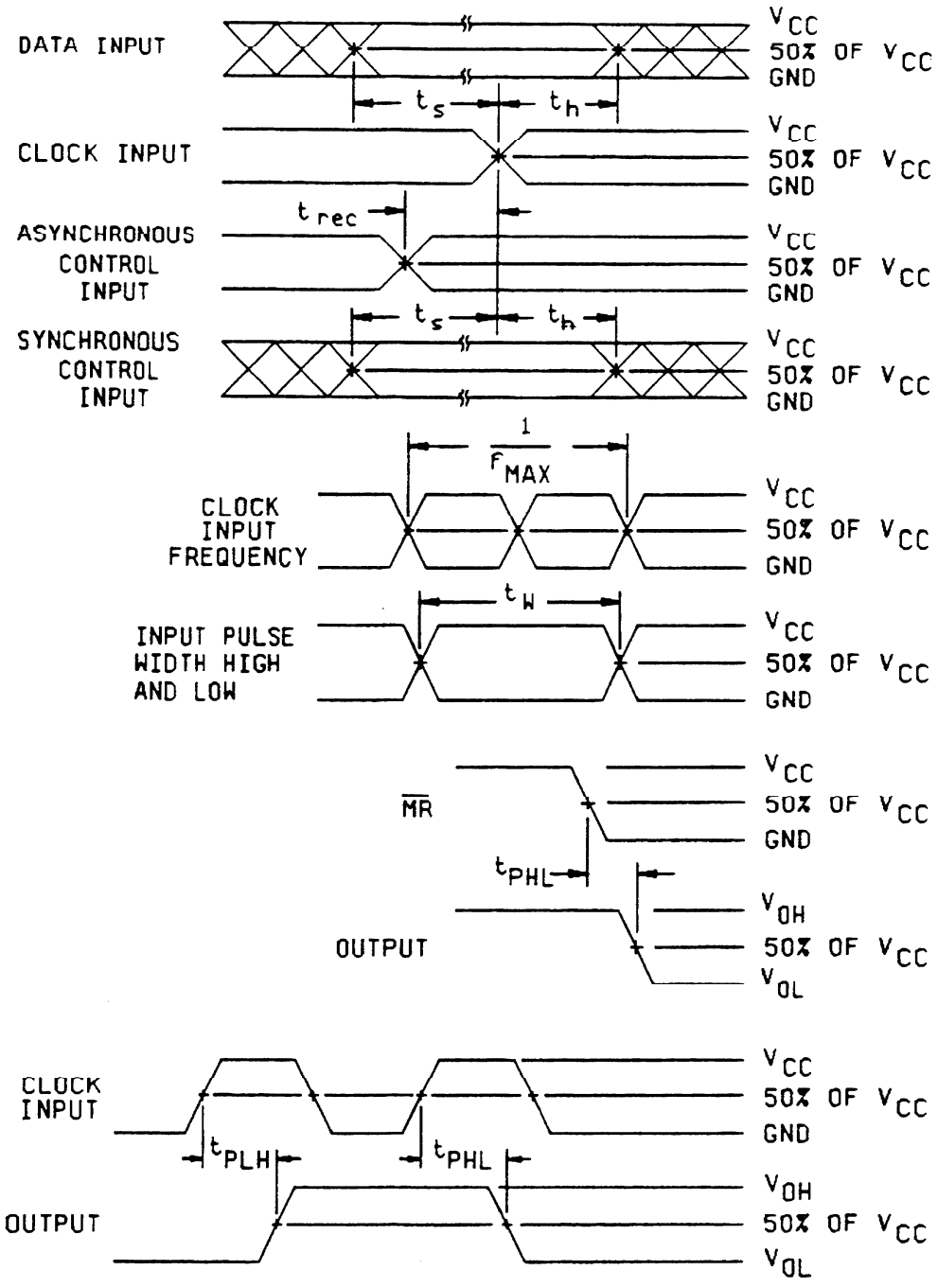
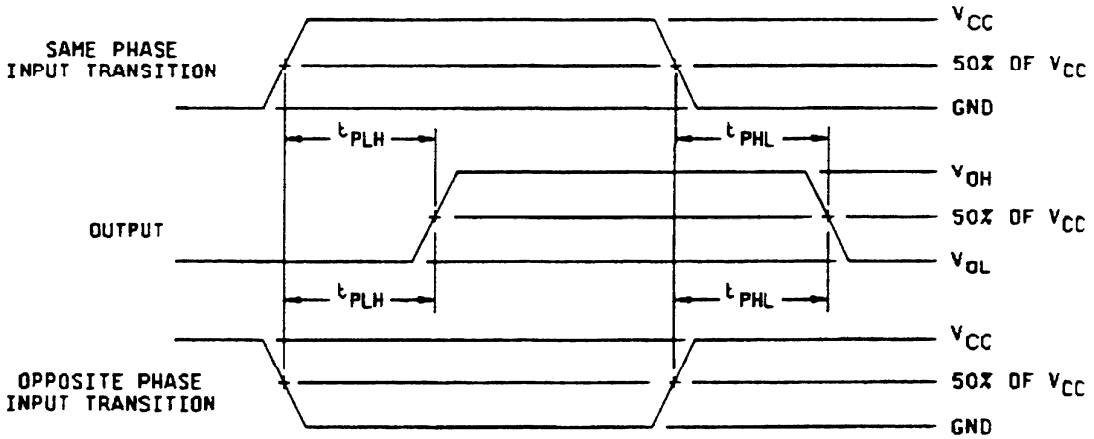
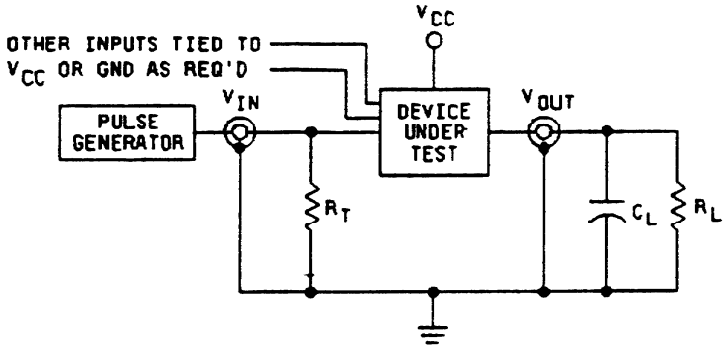


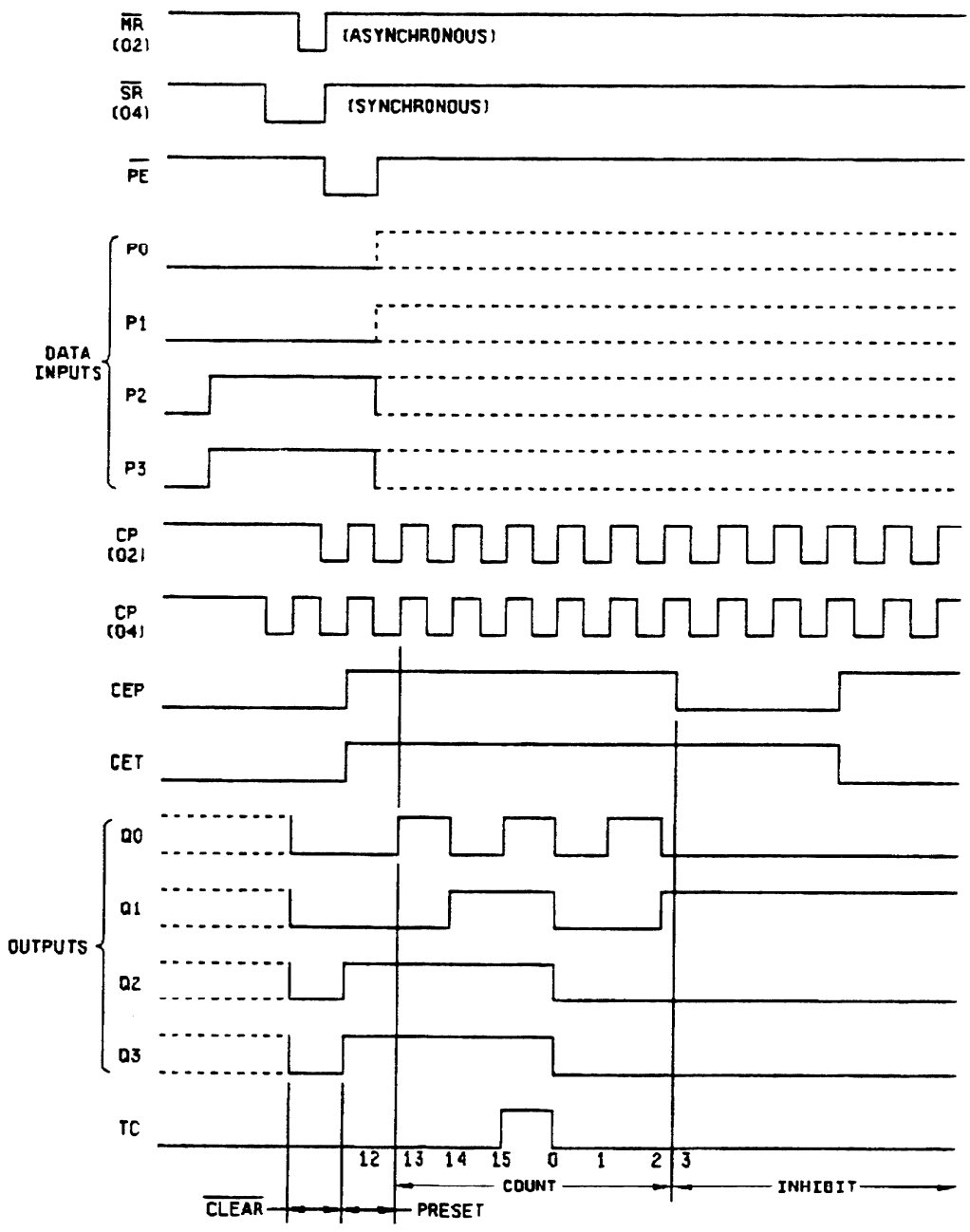
FIGURE 5. Switching time test circuit and waveforms.





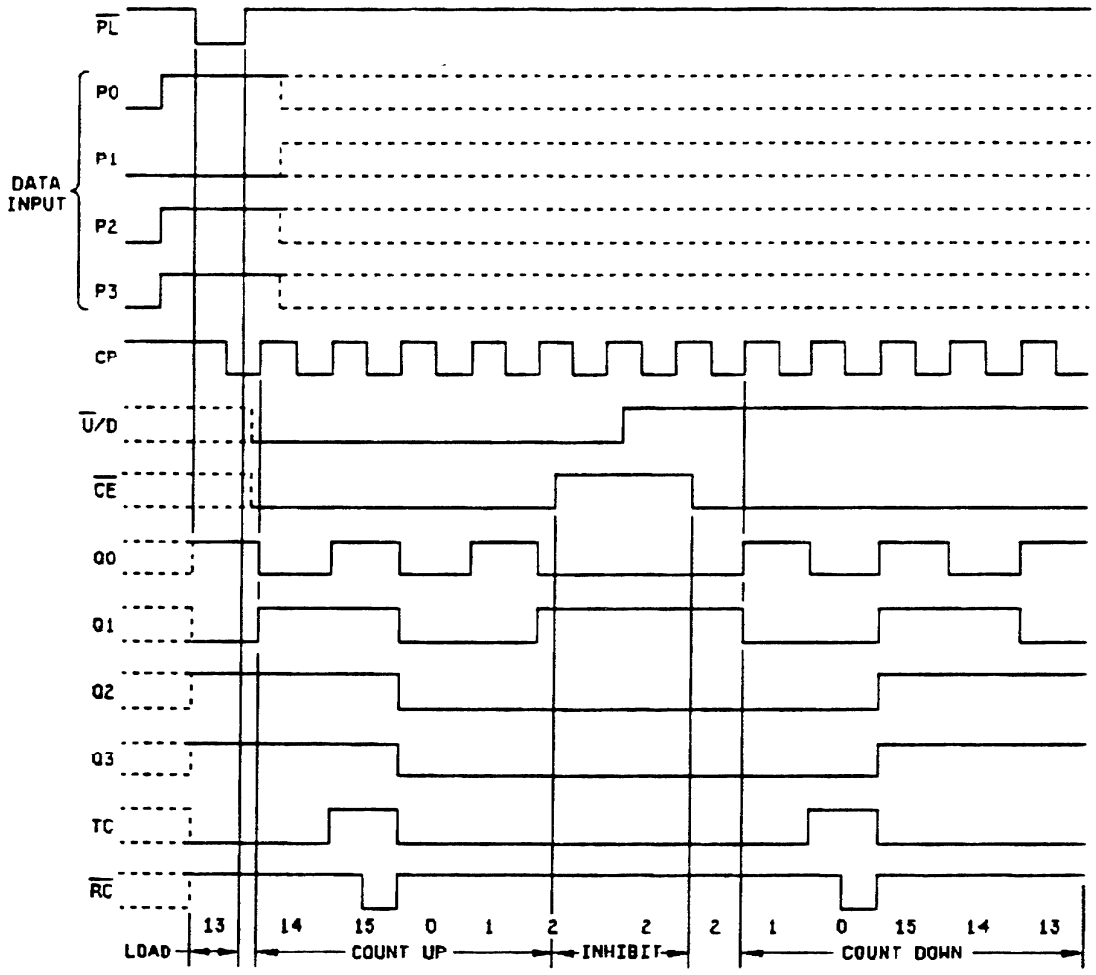
NOTES:
1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_L = 500Ω or equivalent
3. R_T = 50Ω or equivalent.
4. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; duty cycle = 50 percent t_r ≤ 3 ns; t_f ≤ 3 ns; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC}, and 90% of V_{CC} to 10% of V_{CC}, respectively.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.

FIGURE 5. Switching time test circuit and waveforms - Continued.



Device types 02 and 04.

FIGURE 6. Counting sequence.



Device type 05.

FIGURE 6. Counting sequence - Continued.

3.1.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.1.6 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained and available upon request.

3.2 Electrical performance characteristics and postirradiation end-point electrical parameter limits. Unless otherwise specified, the electrical performance characteristics, and postirradiation end-point electrical parameter limits are as specified in table I, and apply over the case operating temperature range specified. Test conditions for these specified characteristics and limits are as specified in table I. A pin for pin conditions and testing sequence for table I parameters shall be maintained and available upon request from the qualifying activity, on qualified devices.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I. Radiation hardness assurance level designators M, D, and R (see MIL-M-38510) in table I are postirradiation end-point electrical parameters.

3.5 Correctness of indexing and marking. All devices shall be subjected to the final electrical tests specified in table II after PIN marking to verify that they are correctly indexed and identified by PIN. Optionally, an approved electrical test may be devised especially for this requirement.

3.5.1 Radiation hardness assurance identifier. The radiation hardness assurance identifier shall be in accordance with MIL-M-38510 and herein (see 3.4).

3.6 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 40 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, except as modified herein.

4.1.1 Burn-in and life test circuits. Burn-in and life test circuits shall be constructed so that the devices are stressed at the maximum operating conditions stated 4.2b or 4.2c as applicable or equivalent as approved by the qualifying activity.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute lines 1 through 7 of table II herein.

b. Static burn-in, test condition A, method 1015 of MIL-STD-883. Test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table I of method 1015 for class B devices.

   1. For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2$ ±0.5 V. Resistors R1 are optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2$ ±0.5 V. R1 = 220Ω to 47 kΩ.

   2. For static burn-in II, all inputs shall be connected through the R1 resistors to V_{CC}. Outputs may be open or connected to $V_{CC}/2$ ±0.5 V. Resistors are optional on open outputs, and required on outputs connected to $V_{CC}/2$ ±0.5 V. R1 = 220Ω to 47 kΩ.

   3. V_{CC} = 5.5 V +0.5 V,-0.00 V.

c. Dynamic burn-in, test condition D, method 1015 of MIL-STD-883.

   1. Input resistors = 220Ω to 2 kΩ ±20 percent.

2. Output resistors = 220Ω ±20 percent.

3. V_{CC} = 5.5 V +0.5 V,-0.00 V.

4. The circuit for device types 02 and 04, is configured as follows. The clock input shall be through a resistor to a clock pulse (CP1). Data load inputs P0 to P3 shall be connected through a resistor in parallel to a common clock pulse (CP2). Load control input PE shall be connected through a resistor to GND. All other inputs shall be connected through a resistor in parallel to V_{CC}. Each output shall be connected through a resistor to $V_{CC}/2$ ±0.5 V.

   The circuit for device type 05, is configured as follows. The clock input shall be through a resistor to a clock pulse (CP1). Count enable control input CE shall be connected through a resistor to GND. All other inputs shall be connected through a resistor in parallel to V_{CC}. Each output shall be connected through a resistor to $V_{CC}/2$ ±0.5 V.

5. CP1, CP2 = 25 kHz to 1 MHz square waves; $f_{CP2} = f_{CP1}/2$; duty cycle = 50 ±15 percent; V_{IH} = 4.5 V to V_{CC}; V_{IL} = 0 V ±0.5 V; t_r, $t_f \leq 100$ ns.

d. Interim and final electrical parameters shall be as specified in table II herein.

e. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.1 Percent defective allowable (PDA). The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

a. Static burn-in I and II failures shall be cumulative for determining the PDA.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for static burn-in. Dynamic burn-in is not required.

c. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified devices times 100 divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510, and 4.3.1 herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E, inspections (see 4.4.1 through 4.4.5).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. Only those device types that pass ESDS testing at 2,000 volts or greater shall be considered as conforming to the requirements of this specification. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be performed in accordance with table II herein.

b. O/V, O/I (latch-up) tests and $V_{GBL/H}$ (ground bounce) tests shall be measured only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up test shall be considered destructive. Test all applicable pins on 5 devices with no failures.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. Test all applicable pins on 5 devices with no failures.

d. Subgroups 9 and 11 shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.

e. Subgroups 7 and 8 tests shall be sufficient to verify truth table.

f. f_{MAX} shall be measured only for initial qualification and after process or design changes which may affect the device frequency. Test all applicable pins on 22 devices with no failures.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II, method 5005 of MIL-STD-883 and as follows:

a. Class S steady-state life (accelerated) shall be conducted using test condition D, method 1005 of MIL-STD-883 and the circuit described in 4.2c herein, or equivalent as approved by the qualifying activity.

b. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table III herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III, method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table III herein.

b. Steady-state life test (method 1005 of MIL-STD-883) shall be conducted using test condition D and as specified in 4.5.2 herein using a circuit as described in 4.2c herein, or equivalent as approved by the qualifying activity.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV, method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for device types intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B and S shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes B and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

d. RHA test for device classes B and S for levels M, D, and R shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

e. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified Group A electrical parameters in table I for subgroups specified in table II herein.

f. For device classes B and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Inputs tested high, V_{CC} = 5.5 V dc ±5%, R_{CC} = 10Ω ±20%, V_{IN} = 5.0 V dc ±5%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

b. Inputs tested low, V_{CC} = 5.5 V dc ±5%, R_{CC} = 10Ω ±20%, V_{IN} = 0.0 V dc ±5%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.5.1.1 Accelerated aging test. Accelerated aging shall be performed on class B and S devices requiring an RHA level greater than 5 krads (Si). The post-anneal end point electrical parameter limits shall be as specified in table I herein and shall be the preirradiation end point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cool down procedures. When the burn-in and life tests are completed and prior to removal of bias voltages, the devices under test (DUT) shall be cooled to within 10°C of their power stable condition at room temperature; then, electrical parameter end-point measurements shall be performed.

4.5.3 Quiescent supply current. When performing quiescent supply current measurements (I_{CC}), the meter shall be placed so that all currents flow through the meter.

4.6 Data reporting. When specified in the purchase order or contract, a copy of the following data, as applicable, shall be supplied.

a. Attributes data for all screening tests (see 4.2) and variables data for all static burn-in, dynamic burn-in, RHA tests and steady-state life tests (see 3.4).

b. A copy of each radiograph.

c. The quality conformance inspection data (see 4.4).

d. Parameter distribution data on parameters evaluated during burn-in (see 3.4).

e. Final electrical parameters data (see 4.2d).

f. RHA delta limits.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

TABLE II. Burn-in and electrical test requirements.

Line no.	Applicable tests and MIL-STD-883 test method	Class S device 1/			Class B device 1/		
		Reference paragraph	TABLE I sub-groups 2/	TABLE III delta limits 3/	Reference paragraph	TABLE I sub-groups 2/	TABLE III delta limits 3/
1	Interim electrical parameters (method 5004)	4.2d	1			1	
2	Static burn-in I (method 1015)	4.2b 4.5.2	Required 4/			Not required	
3	Same as line 1	4.2d	1	Δ	4.2d		
4	Static burn-in II (method 1015)	4.2b 4.5.2	Required 4/		4.2b 4.5.2	Required 5/	
5	Same as line 1	4.2d	1*	Δ	4.2d	1*	Δ
6	Dynamic burn-in (method 1015)	4.2c 4.5.2	Required 4/			Not required	
7	Same as line 1	4.2d	1	Δ			
8	Final electrical parameters (method 5004)		1*,2,7*,9			1*,2,7,9 5/	
9	Group A test requirements (method 5005)	4.4.1	1,2,3,4, 7,8,9,10, 11		4.4.1	1,2,3,4, 7,8,9,10, 11	
10	Group B end-point electrical parameters (method 5005)	4.4.2	1,2,3,7, 8,9,10,11	Δ			
11	Group C end-point electrical parameters (method 5005)				4.4.3	1,2	Δ
12	Group D end-point electrical parameters (method 5005)	4.4.4	1,2,3		4.4.4	1,2	
13	Group E end-point electrical parameters (method 5005)	4.4.5	1,7,9		4.4.5	1,7,9	

1/ Blank spaces indicate tests are not applicable.
2/ * indicates PDA applies to subgroup (see 4.2.1).
3/ Δ indicates delta limit shall be required only on table I subgroup 1, where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).
4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters(group A, subgroup 1), in accordance with test method 5004 of MIL-STD-883. For preburn-in and interim electrical parameters the read-and-record requirements are for delta measurements only.
5/ The device manufacturer may at his option either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias) or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in tests (first interim electrical parameters test in table II).

TABLE III. Delta limits at 25°C.

Parameter	Device type	Limits
I_{CCH}, I_{CCL} 1/	All	±100 nA

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine deltas (Δ).

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Acquisition requirements. The acquisition documents must specify the following:

a. Title, number, and date of the specification.

b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1 and 2.2).

c. Complete PIN.

d. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

e. Requirements for certificate of compliance, if applicable.

f. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

g. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

h. Requirements for product assurance and radiation hardness assurance options.

i. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements shall not apply to direct purchase by, or direct shipment to the Government.

j. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_{IN} - - - - - - - - - - - - - - Input terminal-to-GND capacitance
GND - - - - - - - - - - - - - - Ground zero voltage potential
I_{CCH} - - - - - - - - - - - - - Quiescent supply current, outputs high
I_{CCL} - - - - - - - - - - - - - Quiescent supply current, outputs low
I_{IL} - - - - - - - - - - - - - - Input current low
I_{IH} - - - - - - - - - - - - - - Input current high
T_C - - - - - - - - - - - - - - - Case temperature
T_A - - - - - - - - - - - - - - - Ambient temperature
V_{CC} - - - - - - - - - - - - - - Positive supply voltage
C_{PD} - - - - - - - - - - - - - - Power dissipation capacitance
V_{IC} - - - - - - - - - - - - - - Positive input clamp voltage
V_{GB} - - - - - - - - - - - - - - Ground bounce voltage
O/V - - - - - - - - - - - - - - - Latch-up over-voltage
O/I - - - - - - - - - - - - - - - Latch-up over-current
t_w - - - - - - - - - - - - - - - Trigger duration (width)

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise

specified, microcircuits acquired for Government logistic support will be acquired to device class S for National Aeronautics and Space Administration or class B for Department of Defense (see 1.2.2), lead finish C (see 3.3). Longer length leads and lead forming shall not affect the PIN.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges, postirradiation performance or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01*	54AC160
02	54AC161
03*	54AC162
04	54AC163
05	54AC191
06*	54AC192
07*	54AC193
08*	54AC390
09*	54AC393
10*	54AC4017
11*	54AC4020
12*	54AC4024
13*	54AC4040

* These device types to be included in a later revision of this specification.

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static build-up. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Do not handle devices by the leads.

d. Avoid use of plastic, rubber, or silk in MOS areas.

e. Maintain relative humidity above 50 percent, if practical.

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17
NASA - NA

Review activities:
Army - AR, MI, SM
Air Force - 19, 85, 99
DLA - ES
Navy - AS, CG, MC, OC, SH

Preparing activity:
Air Force - 17

Agent:
DLA - ES

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